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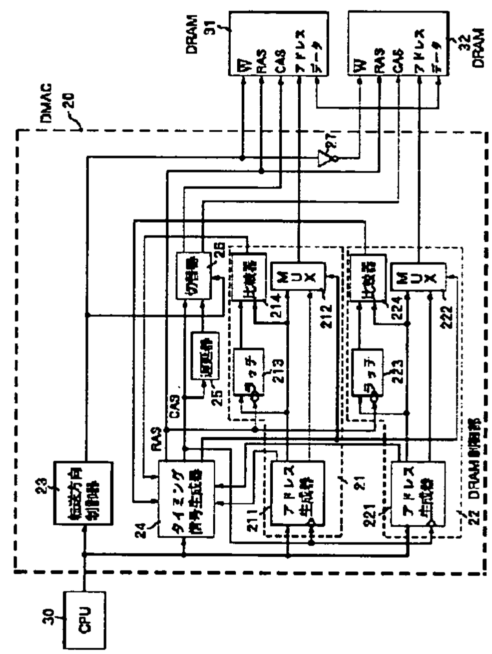
(54) **DMA CONTROLLER**



(57) Abstract:

PURPOSE: To provide the DMA controller which can more accelerate data transfer speed by simultaneously executing both continuous access and simultaneous read/write execution.

CONSTITUTION: According to a data transfer starting instruction from a CPU 30, a timing signal generator 23 latches a row address by using latches 213 and 223 and afterwards, MUs 212 and 222 are switched to the side to output a column address. The timing signal generator 24 lets an output CAS signal fall and outputs data from a transfer source DRAM. A CAS signal delayed for prescribed time by a delayer 25 is inputted through a switcher 26 to a transfer destination DRAM and with the fall of that CAS signal, the data are written. Since the CAS signal is repeatedly turned to L and H levels while holding a RAS signal at the L level, page mode access is performed.